A THEORETICAL APPROACH TO REDUCING SIZE, WEIGHT AND POWER REQUIREMENTS IN FUTURE AIRBORNE TELEMETRY APPLICATIONS THROUGH A NEW IC DESIGN STANDARD

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ABSTRACT

The Defense and Military communities are being faced with increasing pressure to incorporate advanced dynamic data acquisition systems that support space-restrictive environments such as unmanned aerial vehicles while satisfying ever-demanding communications, electronics, measurement and signal intelligence requirements imposed by governmental bodies in response to an increasingly hostile world. This trend is prompting great interest in processors, field programmable gate arrays and electronic memory devices that can withstand these demanding application requirements while exhibiting optimized size and weight characteristics as well as minimized power requirements.

To keep pace, equipment manufacturers have responded with multi-function systems, based on single-board computers (SBCs) in PCI and VME form factors. However, many organizations now foresee an impending limit on the functionality capabilities of currently available board technologies. This paper outlines a new strategic approach in dealing with impending technological obsolescence through the development of a new, open integrated circuit board standard that would improve performance while reducing the cost and complexity of currently available technologies.

KEY WORDS
BFX, SWaP, PHM, Data Acquisition, Data Processing, Telemetry

INTRODUCTION

With rising geopolitical tensions, military and government organizations expect cost-effective, reliable extraction of mission-critical information out of increasingly smaller airborne telemetry system elements. This trend toward smaller form factors is expected to continue, unabated, for the next 50 years. To cost-effectively meet these requirements, research has been initiated by DSPCon engineers in conjunction with partners and clients in the military and commercial sectors to develop a new, Integrated Circuit Board design standard which could provide the foundation for a wide range of embedded telemetry systems that could be successfully utilized in a number of space-restrictive, military and commercial applications for years to come. Initial design of the new standard, code-named BFX, will be presented as a disruptive technology
approach to improve the flexibility and performance of SWaP (size, weight and power) constrained application areas including signal intelligence, radar, sonar, software defined radio, manpack tactical radio and UAVs.

Current IC design approaches utilized throughout the electronics industry focus on putting many functions on large cards, such as Single Board Computers (SBCs) in which processors, programmed logic, I/O and archiving functions are assembled on a single board. This approach is a continuation of past trends to place many functions on a single board due to the need for reliable, high bandwidth communications between the individual electronic components. In newer designs, these functions are almost completely connected using Giga-bit links such as PCI Express. While still satisfactory for a number of current applications, in general, these boards have more functions than most users require, and up to 50% of the board may not be utilized for a given application, which, in many cases, increases the power requirements for any integrated system. As such, this limits the designer’s ability to shrink the footprint of the system as well as complicating heat removal issues.

Additionally, commercial-off-the-shelf (COTS) hardware is still widely used to integrate many applications that require low volume and high mix hardware configurations such as ruggedized military applications using conduction cooled boards in VME, cPCI, and REDI form factors. While this has been an adequate solution for vehicles which have a lot of space to house a system, a growing number of military applications require higher processing capabilities in much smaller telemetry components that can be carried by a soldier on a battlefield (manpack) or carried inside of a small unmanned aircraft, ground vehicle or boat. In all these cases, reduced component size, weight and power consumption have become critical issues, as these systems may have to run from battery power.

For many current SWaP-optimized applications, the prevalent design approach in the industry remains based on the 3U VPX and 3U Compact PCI standards\(^1\). However, due to inherent physical limitations, it is believed an alternative approach could represent significant improvement in space and power requirements along with an improved economic profile over time. This is the essence of BFX.

BFX is envisioned to be a modular design approach composed of “function-specific”, electronic boards, each of which may contain some combination of processors, programmed logic, Input/Output (I/O) or data archiving functions, that must operate within specified size, weight and power limits, use a standardized I/O fabric, and, for military applications, be rugged enough to meet military standards for temperature, shock and vibration. Electronic boards that meet the BFX design criteria will be able to be stacked, side-by-side for unlimited expandability. High speed I/O functionality means that boards can be seamlessly interfaced in any given application. Development of the BFX design rules will not only be compatible with state-of-the-art COTS hardware of today, but will accommodate future developments as well and will be made available to the industry as an open standard. As long as the BFX standards for SWaP and I/O are met, any new electronic boards and associated capabilities will be compatible and should easily integrate into an entire, BFX-based system. A diagram of a proposed BFX standard electronic board is shown in Figure 1. By incorporating these new design rules, the same, larger form factor boards currently utilized in current SWaP-optimized applications could be assembled
using smaller form factor modules which, when put side-by-side, would take up less than one quarter the amount of space currently required. Deployment of such a design strategy could also provide a savings of up to 50% on power because the smaller chassis would only contain the functions required for each application.

The emphasis on smaller, function-specific boards for meeting SWaP needs, as opposed to large, multi-function boards, is one of the key design components of the new BFX paradigm. The standard is essentially a building-block approach where the blocks are small footprint, function-specific, modular (plug-and-play) boards, which, due to their small footprint and low power dissipation requirements, can be stacked side-by-side with a tight board pitch. These function-specific, boards will communicate over a high-speed serial I/O backplane fabric operating at >5GHz bandwidth (e.g. PCI Express). The use of a high-speed serial I/O fabric for inter-board communications will eliminate the need for complicated intra-board routing, allowing the flexibility to shrink the board footprint. Individual cards will be coupled to a high speed backplane with a low cost connector based on a rugged, reinforced version of a PCI express connector, currently used on every PC manufactured in the world. This new approach will provide the system designer flexibility to use only the functions needed for a given application, minimizing wasted space and thereby reducing both size and cooling requirements. These “relaxed” cooling requirements will allow the boards to be placed closer together, further reducing the volume occupied by a system. Due to design improvements, it is anticipated that BFX-based systems will have lower initial costs for system deployment, while allowing greater flexibility for upgrades as system requirements evolve. System upgrades will be in the form of adding greater capacity (e.g. additional processing capability or more system memory) or by integrating newer, more capable electronic functions that will be integrated into boards that meet the BFX standard.
The BFX-based standard board is being designed to feature a small footprint (4”x4”), limited power dissipation (<100W per board), a smaller board pitch (0.5”) and use light metals such as aluminum or, possibly, magnesium (33% lighter than aluminum) for conduction cooling. For telemetry applications that are air-cooled, BFX-based components are being designed with a board pitch that will be somewhat larger. The weight of a single BFX board, including the metal required for conduction cooling, has a design target of less than 0.5 lbs. While future trends are indicating that lower power chips will become available, currently available boards with higher power dissipation requirements will be housed in a multi-slot board (additional metal mass) compatible with the proposed BFX standard board pitch.

As technology progresses, processors, FPGAs and I/O that require less power and provide more performance will become increasingly important. It is anticipated in the next 5 years that power consumption is going to drop by a factor of 10 as the electronics industry supports more compact telemetry devices for use by the defense sector. The design approach of the BFX standard anticipates this industry-wide trend and will take advantage of the goal of reducing power usage in all aspects of the electronic circuitry.
In the remaining sections of this paper, the proposed BFX standard will be compared with current industry standards highlighting anticipated advantages of the new design paradigm. Current industry standards to which BFX will be compared include 3U VPX (VITA 46 standard and ruggedized VITA-48 or REDI standard) and PC-104+.

PROPOSED PHYSICAL DIMENSIONS: FORM FACTOR AND BOARD SPACING

The form factor design goal for the BFX-based boards has been selected to be 4”x4” which is smaller than current single board computer standards such as 3U VPX (4”x7”) or 6U VPX (7”x9”), but is comparable in size to PC/104+ (4”x4”) which is currently used in a majority of PC’s and some applications where SWaP is critical. The spacing of the BFX boards was chosen to be an aggressive 0.5 inches to better accommodate current and anticipated conduction cooling requirements.

Figure 2 illustrates a comparison of footprint size among currently available board standards and BFX. Both the 6U-VPX and 3U-VPX standards are Single Board Computers (SBC), containing many functions, as opposed to proposed BFX boards that will be function-specific. The 3U-VPX standard was chosen by the electronics industry as a smaller version of the 6U-VPX standard to meet SWaP needs in the military and commercial sectors. The current design approach in the electronics industry is based on the 3U VPX standard in which the typical footprint of a SBC is 4”x7”, the board pitch standard is 0.8” (1” if the board is ruggedized according to the VITA-48 REDI standard) and the individual boards typically weigh on the order of 0.8 lbs or more. The older PC/104+ standard has a board spacing of 0.662” and uses a stack-through connector approach. This stack-through approach will be eliminated in the BFX-based design, resulting in a smaller volume. In addition, PC/104 requires that one of the boards be a motherboard controller for the other boards in the stack, impacting the total volume of a given system. The BFX approach will have no such requirement for a motherboard controller.

![Figure 2: Comparison of Footprints for BFX and VPX Standards](image-url)
For a given system design, BFX may actually require more of the smaller footprint, function-specific boards to distribute the data processing and heat removal load than a comparable single board computer approach, but due to its aggressive board spacing, the overall size and volume of a BFX-based system should be smaller than those developed using the 3U-VPX standard as no space and power will be wasted by SBC functions that are not used. It is anticipated that a typical BFX-based airborne telemetry system design will involve 4 to 8 BFX boards. The size of a chassis-mounted system with conduction cooling is anticipated to be 4”x4”x1.6” for four BFX boards and 4”x4”x3.2” for eight BFX boards.

**BFX WEIGHT**

The BFX design standard outlines total board weight to be no greater than 0.5 lbs based on the amount of metal required for the heat removal by conduction cooling. When including the chassis, we must also include the weight of the cold plate. For a typical 4 to 8 BFX board chassis mounted system, the weight of the system is anticipated to be between 3.2 and 6.4 lbs. For a BFX based system design, there is no wasted space on the boards and therefore no excess weight due to unused components/functions.

**BFX INPUT/OUTPUT (I/O) COMMUNICATIONS**

High-speed serial I/O standards, such as PCI Express, allow the reduction of intra-board routing connections within several functions on a given board to routing of data and control signals via a high speed serial I/O fabric or point-to-point interface. This simplifies board design and helps to minimize the amount of space used. Adopting a concept from one of the newer standards, VPX, the design of BFX-based boards will almost exclusively use high-speed serial links for all data traffic communications. Additionally, entire BFX-based systems should be easy to produce due to planned incorporation of a small I/O connector which will be able to handle greater than 32, 5+ Gbit links that will be routed through a very low-cost, easy-to-build backplane. This design strategy will require minimal need for contacts to the backplane, and should allow designers to use COTS standards for communicating between processors, and programmable logic. Targeted supported Protocols include PCI Express, Serial FPDP, Vita 41 Aurora, Fibre Channel, Ethernet, and USB. It is expected that designers will generally use PCI Express and Ethernet for processor cards; however, PCI Express should continue to be preferred since it takes less hardware area to implement for modern processors because it is essentially built-in. The BFX I/O connector will be able to handle up to 32, 5+ Gbit/s link and all links will be point-to-point with a characteristic impedance of 100 Ohms.
The proposed strategy for a BFX ruggedized connector is to use a reinforced PCI express connector on a backplane for each I/O card with very aggressive card spacing (0.5”). PCI Express connectors are currently used on every PC manufactured in the world. Cards that can be conduction cooled and have a small form factor could also exist as a single slot or multi-slot solution for units that require significant heat dissipation or have circuit height issues. This same strategy has been used for PCMCIA cards that go inside of laptop PCs.

When compared to the industry-common but older PC/104+ board standard which has a comparable footprint (4”x4”), the proposed BFX standard will provide superior bandwidth (>5 Gbytes) through the use of the PCI Express serial I/O standard. Additionally, in PC/104+ systems, the boards are limited in terms of how many can be stacked together (typically up to a maximum of four boards) because the signaling requirements between boards cannot be maintained. For the BFX standard, a high-speed, robust I/O places little limitation on how many boards (and therefore functions) can be stacked in a given chassis, making expandability easy. It is also noteworthy that PC/104+ cannot host PCI Express, due to the bandwidth limitations of the PC/104+ connector.

BFX-based systems will enable a cost effective migration strategy to accommodate changing application requirements. Due to function-specific, space- and weight- optimized component design that will eliminate any and all extraneous functionality, initial installation costs should be significantly lower, as future upgrades will be now relegated to simple plug-and-play modular additions. This design strategy should promote substantially longer system life without the need for major system redesigns in the face of more aggressive system application requirements.

CONCLUSION

A new paradigm for electronic boards, BFX, is being developed to meet increasingly demanding airborne telemetry applications in space-constrained environments. The BFX approach should not only addresses the SWaP needs of the military and commercial world for many years to come, but will also provides designers the flexibility to develop high performance systems that can meet expanding mission requirements and new technological developments in the electronics industry.

REFERENCES